12.4 A 7.5Gb/s 10-Tap DFE Receiver with First Tap Partial Response, Spectrally Gated Adaptation, and 2nd-Order Data-Filtered CDR

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As serial links push to higher data rates, more sophisticated equalization schemes are required to counter the effects of ISI. DFE is favored to cancel post-cursor ISI since it does not amplify noise or reduce received signal strength. Furthermore, it is necessary in today's backplanes for the DFE to automatically adapt to the characteristics of the channel [1]. This paper describes the architecture and circuits to address three important concerns of such DFEs: closing timing to cancel the ISI from immediately preceding bits, ensuring the proper convergence of the adaptation algorithm, and providing in-situ diagnostics capabilities.

It is possible to ease the timing requirement for the first DFE tap by using a partial-response DFE (PrDFE) architecture [2]. By loop unrolling, one can remove the sampler from the decision feedback path. However, the increased data latency due to the PrDFE selection logic subtracts from the timing budget of later DFE taps.

Figure 12.4.1 shows the double-data-rate receiver with partial response (tap 1) and DFE (taps 2 to 10). Two levels of decision feedback are used to close timing despite the aforementioned PrDFE latency. A linear equalizer first amplifies Vin to partially correct for high-frequency channel loss. It also buffers the sampler-bank input capacitance from the channel. The amplified signal is driven to 3 data sampler paths and 2 edge sampler paths per odd/even phase. Two adjustable differential offset preamplifiers (ADOP) sum PrDFE threshold coefficient w_1 to the received signal. The resulting signals are sampled to produce speculative data decisions dPE and dNE, assuming the previous data symbol was +1 or -1, respectively. An "adaptive" sampler, whose output is aE, can be configured to produce an error signal for adaptation or to be swapped with either data sampler for live offset calibration [3]. Sampler swapping is accomplished by a multiplexer immediately following the samplers. Partial response selection is then performed by a succeeding multiplexer.

Once even data symbol, dE, is decided, it is fed back only to the even samplers for 2nd post-cursor cancellation. Current-steering DACs whose outputs are current summed onto the ADOP outputs perform feedback weighting by coefficient w_2. By operating within the half-rate logic domain and avoiding the analog delay of the ADOPs, this local feedback path is able to meet the 266ps timing requirement for the 2nd tap. Such "local" feedback paths exist separately within the even and odd domains. Because these local feedback paths require independent multiplication and summation for each sampler, DFE taps 3 to 10 are implemented with a conventional full-rate architecture.

To minimize latency due to sampler swapping and partial response selection, the multiplexers are implemented with dynamic logic, as shown in Fig. 12.4.2. The precharged sampler outputs are inputs to differential PMOS domino multiplexers. Weak cross-coupled devices act as differential level keepers. An SR latch, conventionally placed directly after the sampler, is instead placed after the multiplexers to store the dynamic outputs at static CMOS levels. This dynamic circuit achieves ~40ps lower latency from dClkE to dE than a static CMOS implementation.

The CDR loop, shown in Fig. 12.4.3, controls 5 clock domains. Partial-response signals are known to have a bimodal jitter distribution that degrades CDR tracking bandwidth when a conventional 2× oversampling bang-bang phase detector (BBPD) is used directly as in [5]. In this work, the BBPD is combined with PrDFE edge sampling and data filtering on 3b patterns to overcome this problem. Data filtering selects the edge sample eP as the timing reference for 110 data transitions and eZ for 101 and 010 data transitions, resulting in a unimodal distribution. These 2 edge samplers capture 75% of random data transitions. A 2nd-order loop is used to improve jitter tolerance (JTOL) in the presence of large frequency offsets, resulting in a complete plesiochronous PrDFE clock-recovery solution. D_os is typically set to provide one-half UI offset between eClk and dClk, while A_os can be programmed to arbitrary phase offsets to allow BER-based eye measurement in plesiochronous links. A separate accumulator for the DFE clock domain along with the selective inversion of the BBPD output allows us to align transitions of the DFE output to the data transitions despite variations in feedback latency. The TX accumulator allows plesiochronous parallel loop-back testing for JTOL, etc.

DFE coefficient adaptation is implemented with the sign-sign LMS (SS-LMS) algorithm. SS-LMS uses relatively simple hardware, but requires the incoming data to be spectrally flat for proper convergence [4]. While data scrambling may satisfy this requirement in some applications, it is not always possible. For example, approximately random data may be interspersed with periods of highly autocorrelated data, such as 8b/10b idle patterns. Halting adaptation when such autocorrelated data is detected prevents erroneous wandering of DFE coefficients.

Spectrally gated adaptation is performed using cross-correlation hardware, shown in Fig. 12.4.4. The deserialized data is periodically captured to provide a snapshot of 14 data bits d_{n-10} to d_{n+3}. These same bits are used in both equalization adaptation and correlation testing to synchronize the two functions. In the correlation test, each pair of bits in the snapshot is checked for equality. The results are accumulated over a sequence of 255 snapshots. After the last snapshot, the magnitudes of the 91 accumulators are compared against a programmable threshold. If any of the cross-correlation magnitudes exceeds the threshold, the SS-LMS update corresponding to the same set of snapshots is rejected. Synthesized adaptation hardware including the SS-LMS engine and cross-correlation logic occupies 99,300μm² in a 90nm process and is shared across 4 to 16 links to amortize the area cost.

Spectrally gated adaptation is demonstrated in Fig. 12.4.5, which shows the adaptation of several DFE taps during periods of random (PRBS-31) and static (10'b 0010010111) data transmitted over an 18-inch backplane link with 2 HM-Zd connectors. When adaptation is not spectrally gated, DFE coefficients drift to incorrect values during the static pattern. When random data returns, the link fails to meet the BER specification of 1E-12 until adaptation recovers. When the cross-correlation hardware is used to gate adaptation, DFE coefficient updates are blocked during the static data period, and link BER is maintained.

Receiver performance is demonstrated in Fig. 12.4.6, which plots sinusoidal JTOL (DJ=0.43UIpp, RJ=0.18UIpp). The CDR tracking bandwidth is ~3MHz and high-frequency JTOL is 0.3UIpp at BER=1E-12. The 2nd-order CDR allows the link to maintain nearly constant jitter tolerance during mesochronous and plesiochronous operation.

The 7.5Gb/s receiver draws 113mA from a 1.2V supply. A complete transceiver with the components shown in Fig. 12.4.7 occupies 760×935μm² in a 90nm CMOS process.

Acknowledgements:
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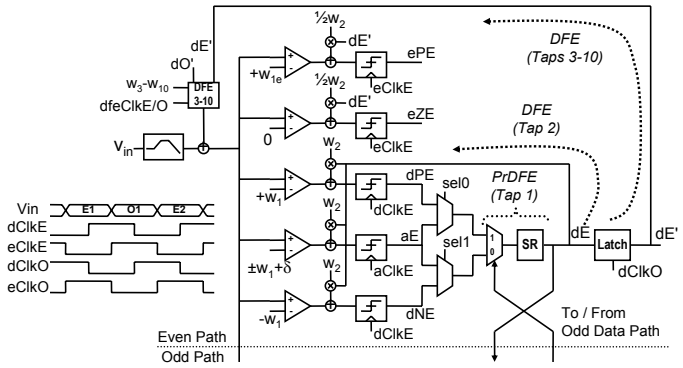

Figure 12.4.1: One phase of double-data-rate RX with PrDFE.

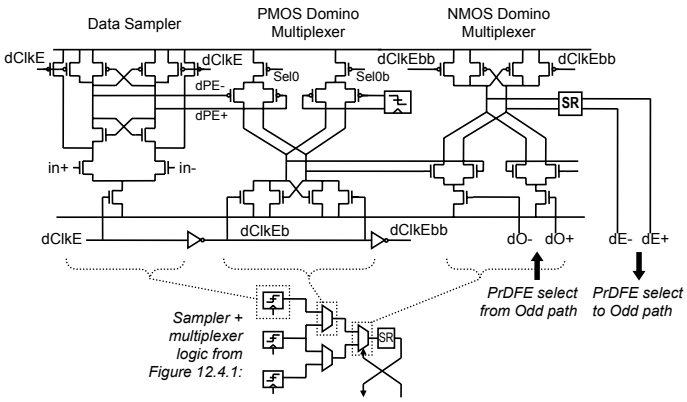

Figure 12.4.2: Sampler (StrongArm) latches directly driving domino multiplexers.

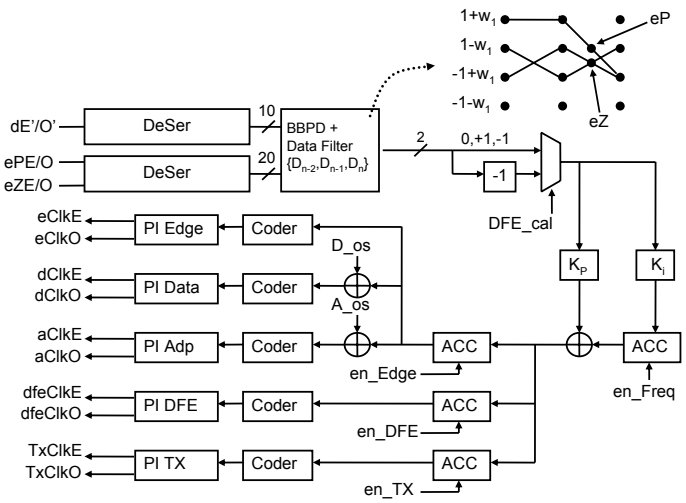

Figure 12.4.3: Second-order CDR with PrDFE data filtering.

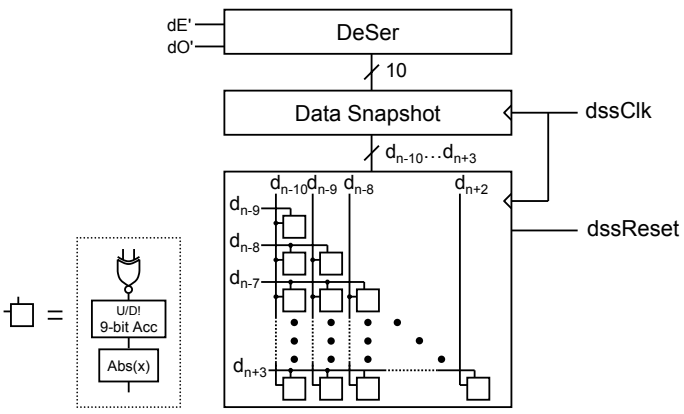

Figure 12.4.4: Data cross-correlation logic.

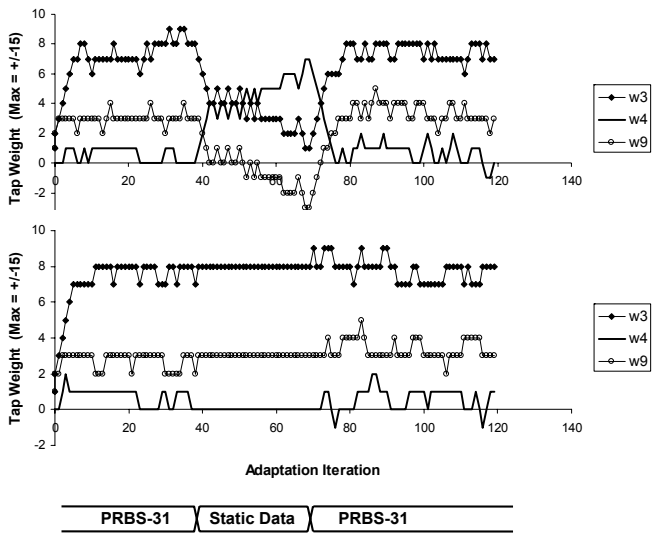

Figure 12.4.5: DFE adaptation without (top) / with (bottom) spectral gating.

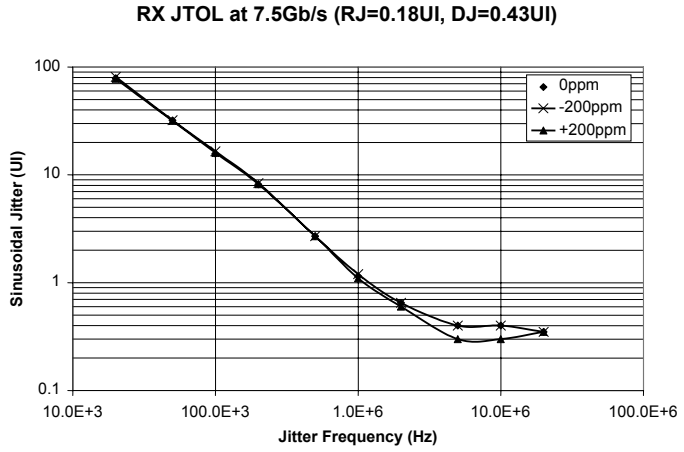

Figure 12.4.6: Measured sinusoidal jitter tolerance at BER=1E-12.

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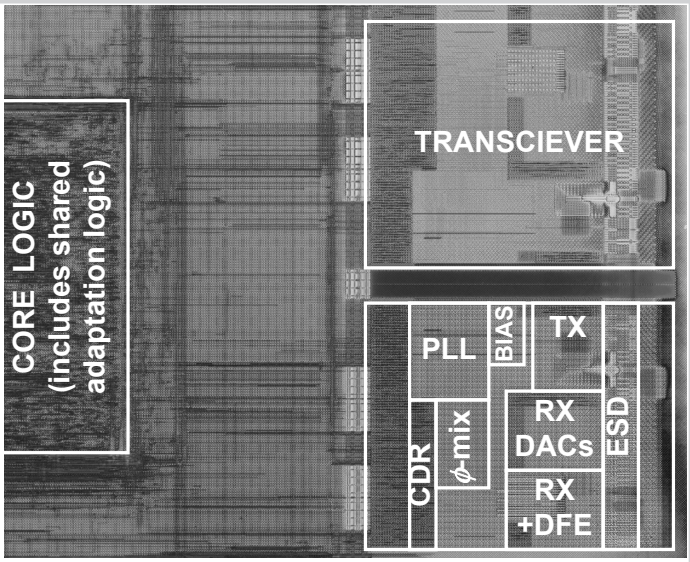

Figure 12.4.7: Chip micrograph (bump + 2 metals removed).

